FAIRCHILD SEMICONDUCTOR®

March 2008

FST3125 — 4-Bit Bus Switch

Features

- 4Ω Switch Connection between Two Ports
- Minimal Propagation Delay through the Switch
- Low I_{CC}
- Zero Bounce in Flow-through Mode
- Control Inputs Compatible with TTL Level

Description

Fairchild switch FST3125 provides four high-speed CMOS TTL-compatible bus switches. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device is organized as four one1-bit switches with separate /OE inputs. When /OE is LOW, the switch is ON and port A is connected to port B. When /OE is HIGH, the switch is OPEN and a high-impedance state exists between the two ports.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FST3125M	-40 to 85°C	14-Lead, Small Outline Integrated Circuit (SOIC) 0.150 inch Narrow	Tube
FST3125MX	-40 to 85°C	14-Lead, Small Outline Integrated Circuit (SOIC) 0.150 inch Narrow	Tape and Reel
FST3125QSC	-40 to 85°C	16-Lead, Quarter Size Outline Package (QSOP) MO-137 0.150 inch Wide	Tube
FST3125QSCX	-40 to 85°C	16-Lead, Quarter Size Outline Package (QSOP) MO-137 0.150 inch Wide	Tape and Reel
FST3125MTC	-40 to 85°C	14-Lead, Thin Shrink Small Outline Package (TSSOP) MO-153, 4mm Wide	Tube
FST3125MTCX	-40 to 85°C	14-Lead, Thin Shrink Small Outline Package (TSSOP) MO-153, 4mm Wide	Tape and Reel

All packages are lead free per JEDEC: J-STD-020B standard.

The Fairchild switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

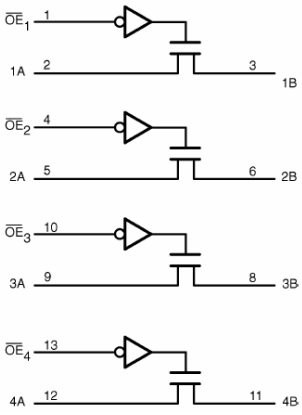


Figure 1. Logic Diagram

Pin Configurations

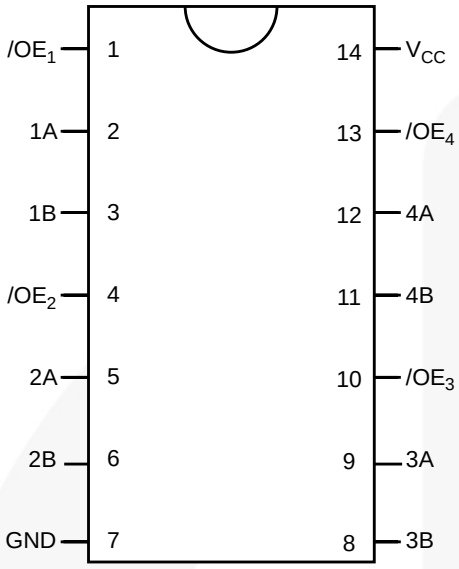


Figure 2. SOIC and TSSOP Pin Assignments

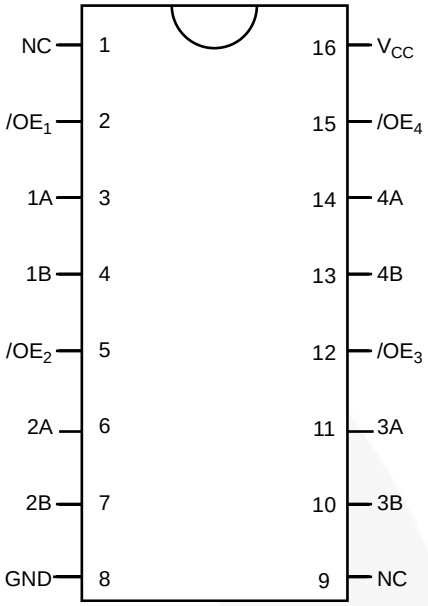


Figure 3. QSOP Pin Assignments

Pin Descriptions

Pin Names	Description
$/OE_1$, $/OE_2$, $/OE_3$, $/OE_4$	Bus Switch Enables
1A, 2A, 3A, 4A	Bus A
1B, 2B, 3B, 4B	Bus B
NC	Not Connected
V_{CC}	Supply Voltage
GND	Ground

Truth Table

Inputs	Inputs/Outputs
/OE	A, B
LOW	A = B
HIGH	High Impedance

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	-0.5	7.0	V
V_S	DC Switch Voltage	-0.5	7.0	V
V_{IN}	DC Input Voltage[1]	-0.5	7.0	V
I_{IK}	DC Input Current		-50	mA
I_{OUT}	DC Output Sink Current		128	mA
I_{CC} / I_{GND}	DC V_{CC} / GND Current		±100	mA
T_{STG}	Storage Temperature Range	-65	+150	°C

Note:

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Power Supply Operating		4.0	5.5	V
V_{IN}	Input Voltage		0	5.5	V
V_{OUT}	Output Voltage		0	5.5	V
t_r, t_f	Input Rise and Fall Time	Switch Control Input[2]	0	5	ns/V
		Switch I/O	0	DC	
T_A	Operating Temperature, Free Air		-40	+85	°C

Note:

2. Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Typical values are at V_{CC} = 5.0V and T_A = 25°C.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=-40 to +85°C			Units
				Min.	Typ.	Max.	
V_{IK}	Clamp Diode Voltage	I_{IN} = -18mA	4.5			-1.2	V
V_{IH}	High-Level Input Voltage		4.0 to 5.5	2.0			V
V_{IL}	Low-Level Input Voltage		4.0 to 5.5			0.8	V
I_{IN}	Input Leakage Current	$0 \le V_{IN} \le 5.5$	5.5			±1.0	µA
I_{OZ}	Off-state Leakage Current	$0 \le A, B \le V_{CC}$	5.5			±1.0	µA
R_{ON}	Switch On Resistance(3)	V_{IN} = 0V, I_{IN} = 64mA	4.5		4	7	Ω
		V_{IN} = 0V, I_{IN} = 30mA	4.5		4	7	
		V_{IN} = 2.4V, I_{IN} = 15mA	4.5		8	15	
		V_{IN} = 2.4V, I_{IN} = 15mA	4.0		11	20	
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND, I_{OUT} = 0	5.5			3	µA
ΔI_{CC}	Increase in I_{CC} per Input	One Input at 3.4V, Other Inputs at V_{CC} or GND	5.5			2.5	mA

Note:

3. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the A or B pins.

AC Electrical Characteristics

T_A = -40 to +85°C, C_L = 50pF, and R_U = R_D = 500Ω.

Symbol	Parameter	Conditions	V_{CC} = 4.5 – 5.5V		V_{CC} = 4.0V		Units	Figure
			Min.	Max.	Min.	Max.		
t_{PHL}, t_{PLH}	Propagation Delay Bus-to-Bus(4)	V_{IN} = Open		0.25		0.25	ns	Figure 4 Figure 5
t_{PZH} ,t_{PZL}	Output Enable Time	V_{IN} = 7V for t_{PZL} V_{IN} = Open for t_{PZH}	1.0	5.0		5.5	ns	Figure 4 Figure 5
t_{PHZ}, t_{PLZ}	Output Disable Time	V_{IN} = 7V for t_{PLZ} V_{IN} = Open for t_{PHZ}	1.5	5.3		5.6	ns	Figure 4 Figure 5

Note:

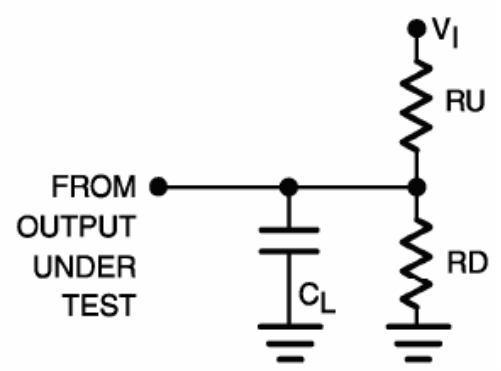
4. This parameter is guaranteed by design, but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical on resistance of the switch and the 50pF load capacitance when driven by an ideal voltage source (zero output impedance).

Capacitance

T_A = +25°C, f = 1MHz. Capacitance is characterized, but not tested.

Symbol	Parameter	Conditions	Typ.	Units
C_{IN}	Control Pin Input Capacitance	V_{CC} = 5.0V	3	pF
$C_{I/O}$	Input/Output Capacitance	V_{CC}, /OE = 5.0V	2	pF

AC Loadings and Waveforms



Notes: Input driven by 50Ω source terminated in 50Ω.
C_L includes load and stray capacitance.
Input PRR = 1.0MHz, t_w = 500ns.

Figure 4. AC Test Circuit

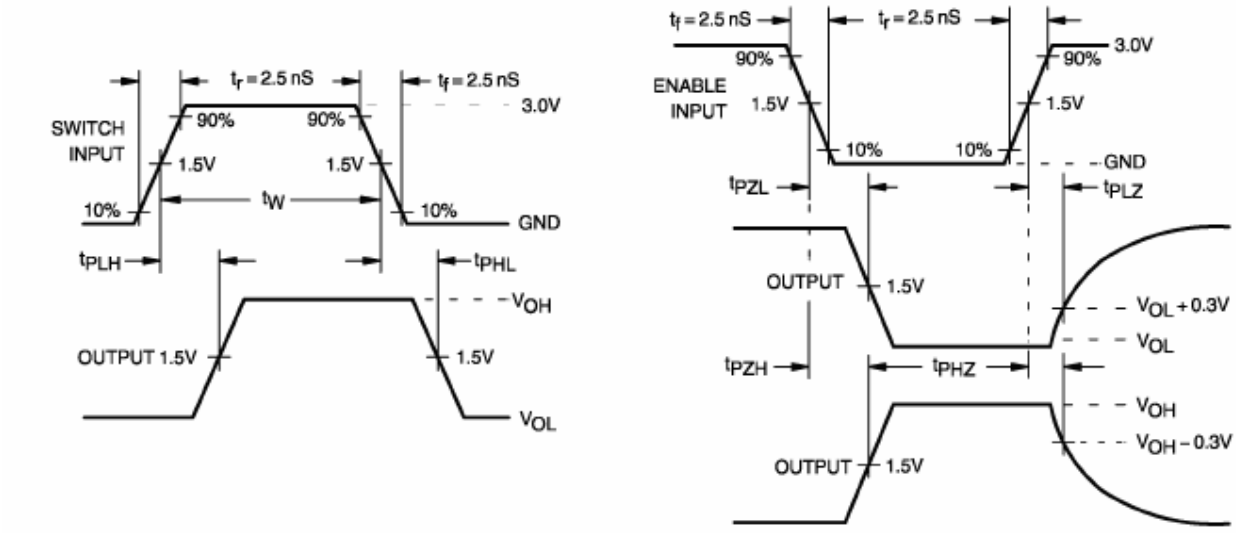


Figure 5. AC Waveforms

Physical Dimensions

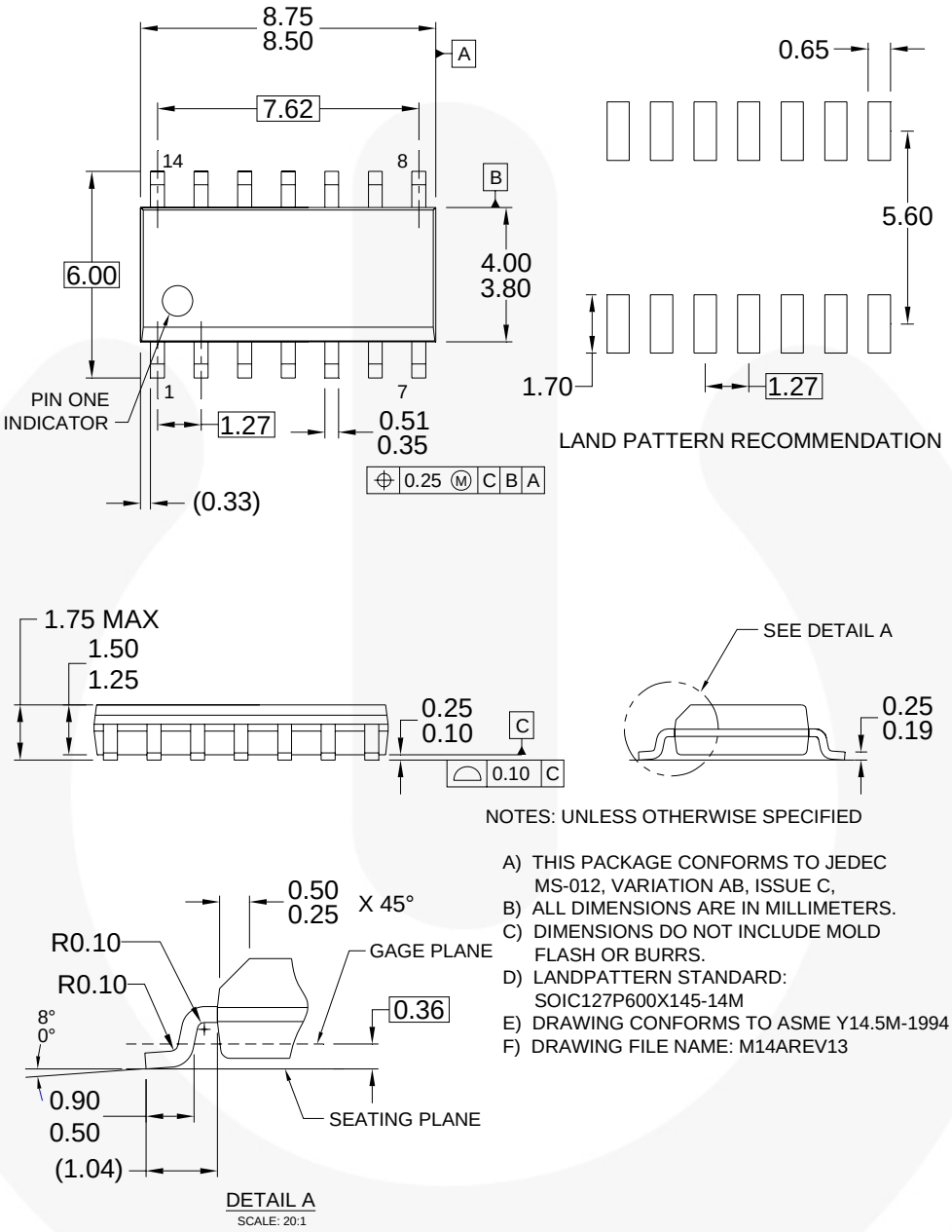


Figure 6. 14-Lead, Small-Outline Integrated Circuit (SOIC) 0.150-inch Narrow

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Physical Dimensions

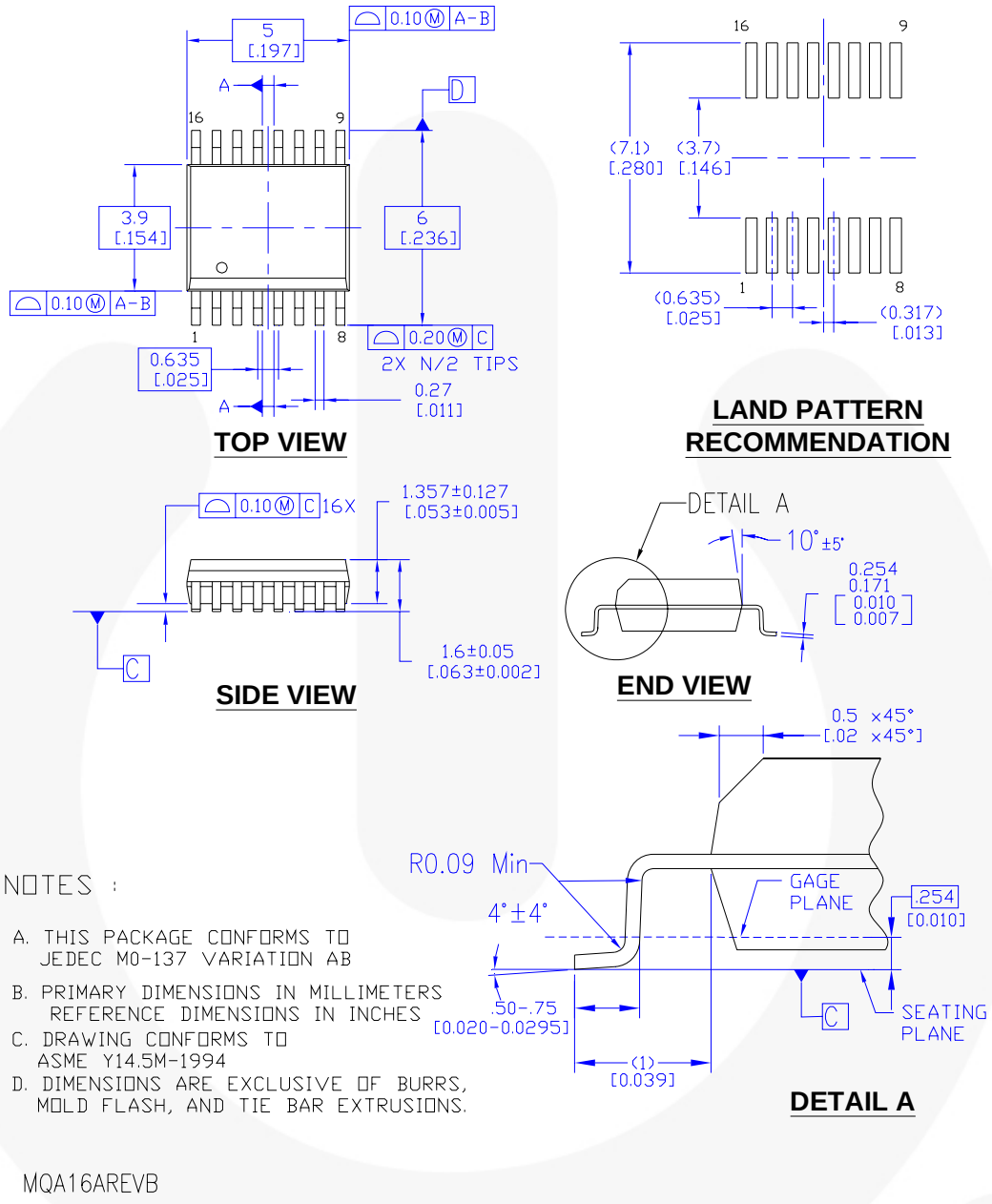

Figure 7. 16-Lead, Quarter-Size Outline Package (QSOP), MO-1370.150-inch Wide

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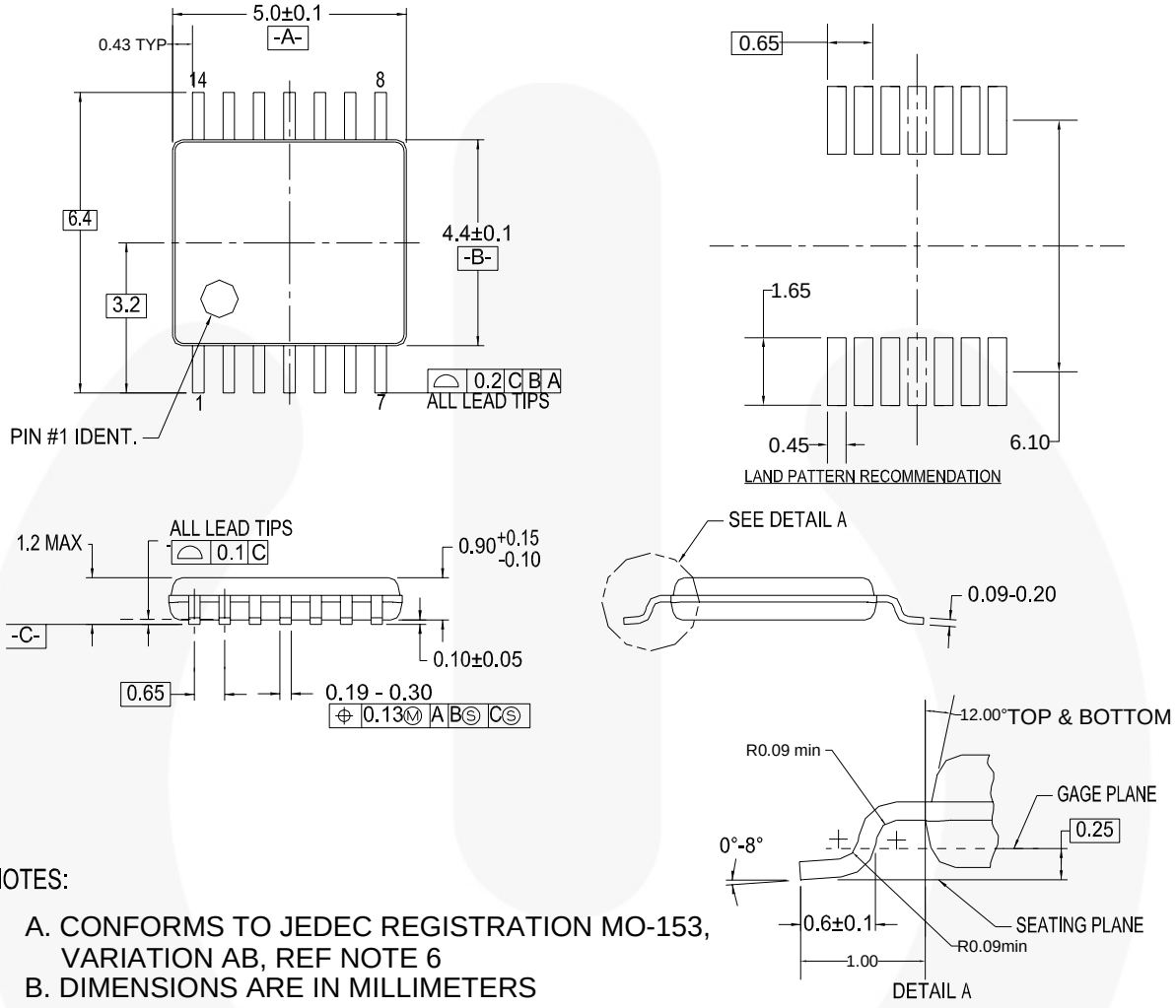
Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6

B. DIMENSIONS ARE IN MILLIMETERS

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

E. LANDPATTERN STANDARD: SOP65P640X110-14M

F. DRAWING FILE NAME: MTC14REV6

Figure 8. 14-Lead, Thin Shrink Small Outline Package (TSSOP) MO-153, 4mm Wide

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